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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,850	12/09/2003	Homero L. Guimaraes	1280-SC12863ZC	4424

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EXAMINER	
FLORES, LEON	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/731,850	GUIMARAES, HOMERO L.	
	Examiner	Art Unit	
	Leon Flores	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-15* is/are allowed.

6)☒ Claim(s) *1-8 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/9/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims (1-8 & 16-18) are rejected under 35 U.S.C. 103(a) as being unpatentable over Baird (US Patent 6,204,787 B1) in view of Ferguson, Jr. et al (hereinafter Ferguson) (US Patent 6,040,793), and further in view of Van Herzeele (US Patent 6,400,295 B1).

2. Re claim 1, Baird discloses a sigma delta converter comprising: an integrator circuitry including an integrator input and an integrator output, wherein an input signal coupled to the integrator input has an input AC voltage component and a DC offset component (In Baird, see fig. 7A: 706 & 707, col. 7, lines 48-50); a pair of capacitors coupled to the integrator input (In Baird, see fig. 7A: 707a & 707b); a first set of switches

coupled the pair of capacitors, the first set of switches configured to transfer a first charge to the pair of capacitors during a first phase, the first charge proportional to a reference voltage (In Baird, see fig. 7B & col. 7, lines 59-61); and a second set of switches coupled to the pair of capacitors. But the reference of Baird fails to specifically disclose the second set of switches configured to transfer the first charge and a second charge to the integrator input.

However, Ferguson does. (See fig. 2: 51 & 56, col. 6, lines 14-17, 29-32, & col. 8, lines 6-9) Ferguson discloses a switched-capacitor sigma-delta analog-to-digital converter having an input and an output and an integrator capacitor connected between the input and output. Before transferring the charge to the integrating capacitors, the input capacitors are charged first by a positive voltage signal and then by a negative voltage signal.

Therefore, taking the combined teachings of Baird & Ferguson as a whole. It would have been obvious to one of ordinary skill in the art to have incorporated a second charge before transferring the charge to the integrator input into the system of Baird, in the manner as claimed, as taught by Ferguson, for the benefit of providing a charge to the input of the integrator at only one interval, instead at two.

The combination of Baird & Ferguson, as discussed above shows the limitations claimed, except they do not specifically disclose the second charge proportional to the DC offset component.

However, Van Herzeele does. (See fig. 2: SC5, fig. 3 & 4, & col. 7, lines 57-67 – col. 8, lines 1-24.) Van Herzeele discloses a fifth switched capacitor with a offset

voltage connected to its input. When switch 1 is close and 2 is open, capacitor C5P is charged by the offset voltage P_{off} and C5N charged to N_{off}. When switch 2 is close and 1 is open, capacitor C5P is charged to N_{off} and C5N charged to P_{off}, and then transferred to the input of the integrator.

Therefore, taking the combined teachings of Baird, Ferguson & Van Herzeele as a whole. It would have been obvious to one of ordinary skill in the art to have incorporated a second charge transfer, proportional to an offset voltage at the input of the integrator, into the system of Baird, as modified by Ferguson, in the manner as claimed, and as taught by Van Herzeele, for the benefit of providing to the modulator offset compensation. (See col. 8, lines 15-18.)

3. Re claim 2, the combination of Baird, Ferguson & Van Herzeele further discloses a comparator coupled to the integrator circuitry output, the comparator including a comparator output. (In Ferguson, see fig. 2: 58 & col. 4, line 48)

4. Re claim 3, the combination of Baird, Ferguson & Van Herzeele further discloses that wherein the integrator circuitry comprises N integrators coupled in series forming an Nth-Order sigma delta loop filter, each of the N integrators having a first input, a second input, a first output and a second output, each of the N integrators having a first integrator capacitor coupled to the first input and the first output and a second integrator capacitor coupled to the second input and the second output. (In Baird, see fig. 4B & col. 6, lines 33-37)

5. Re claim 4, the combination of Baird, Ferguson & Van Herzeele further discloses a comparator coupled to the integrator circuitry output, the comparator including a comparator output (In Ferguson, see fig. 2: 58); a third set of switches coupled to the pair of capacitors, the third set of switches configured to change a polarity of the first charge and the second charge based on the comparator output (In Ferguson, see col. 5, lines 5-12, col. 6, lines 57-67); and a fourth set of switches coupled to the pair of capacitors, the fourth set of switches configured to change a polarity of the second charge based on the comparator output (In Ferguson, see col. 5, lines 5-12, col. 6, lines 57-67), wherein the polarity of the second charge is configured to cancel the DC offset component of the input signal. (In Van Herzeele, see col. 7, lines 57 – col. 8, lines 18.)

6. Re claim 5, the combination of Baird, Ferguson & Van Herzeele further discloses a digital to analog converter coupled to the pair of capacitors for producing the second charge. (In Ferguson, see col. 1, lines 63-64 & col. 4, lines 4-49.)

7. Re claim 6, the combination of Baird, Ferguson & Van Herzeele further discloses that the digital to analog converter configured to receive a multi-bit code word input from a digital signal processor. (In Ferguson, see fig. 2: element 52, which include a DAC, is configured to receive a multi-bit code from element 78 in order to control the switches.)

8: Re claim 7, the combination of Baird, Ferguson & Van Herzeele further discloses that wherein the integrator is a continuous time integrator. (In Baird, see fig. 4B & col. 6,

lines 34-37. Furthermore, since the signal is being integrated three times the signal is converted to digital until the last stage of the 3rd order modulator by a analog-to-digital converter.)

9. Re claim 8, the combination of Baird, Ferguson & Van Herzeele further discloses that wherein the integrator is a discrete time integrator. (In Ferguson, see col. 1, lines 50-56. Furthermore, the output of the integrator is sent to a clocked, latched comparator.)

10. Claim 16 is a method claim corresponding to system claim 1. Hence, the elements in system claim 1 would have necessitated the steps in method claim 16. Therefore, claim 16 has been analyzed and rejected w/r to claim 1.

11. Re claim 17, the combination of Baird, Ferguson & Van Herzeele further discloses comparing an output of a last integrator in the series of integrators to a zero value (In Baird, see fig. 4B. Furthermore, since the comparator located at the end of the third order sigma delta modulator has only one input, therefore, we can say that the other input is grounded.); and determining a polarity of the reference charge in the sum charge based on a result of the comparing. (In Ferguson, see col. 5, lines 8-12)

12. Re claim 18, the combination of Baird, Ferguson & Van Herzeele further discloses that wherein a polarity of the DC offset correction charge in the sum charge is

independent of a result of the comparing. (In Van Herzeele, see col. 8, lines 19-34. Furthermore, the offset charge is dependent on switches controlled by an offset correction signal O_{ffc}, and not on the output of any comparator.)

Allowable Subject Matter

13. Claims 9-15 are allowed.

14. The prior art of record fail to anticipate the respective claim combinations together and nor the respective claim combinations be obvious with the following limitations as claimed:

15. Re claim 9, the further limitations of *"A radio frequency (RF) signal receive path comprising: an intermediate frequency amplifier (IFA) including an IFA output; a plurality of anti-aliasing filters (AAFs) coupled to the IFA output, the AAFs having an AAF output; and a sigma delta converter coupled to the AAF output, the sigma delta converter comprising: integrator circuitry including an integrator input and an integrator output, wherein an input signal coupled to the integrator input has an input AC voltage component and a DC offset component; a pair of capacitors coupled to the integrator input; a first set of switches coupled the pair of capacitors, the first set of switches configured to transfer a first charge to the pair of capacitors during a first phase, the first charge proportional to a reference voltage; and a second set of switches coupled to the pair of capacitors, the second set of switches configured to transfer the first charge and*

a second charge to the integrator input, the second charge proportional to the DC offset component". Claims 10-15 depend on claim 9.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LF
February 15, 2007

David C. Payne
DAVID C. PAYNE
PRIMARY PATENT EXAMINER